AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) The semiconductor integrated circuit according to claim 3 further comprising:

a comparator comparing a value of data read from each memory cell connected to an activated word line with an expected value to be read from said each memory cell, for each column in a test mode; and

an error register accumulatively holding error data based on a comparison result by said comparator, wherein

each bit of said error data indicates ~~said~~ a comparison result by said comparator for a corresponding column, and

said each bit takes a first logical value when said comparison result for said corresponding column always indicates equality whichever word line is activated, and takes a second logical value when once said comparison result for said corresponding column indicates difference.

2. (Canceled)

3. (Currently Amended) A semiconductor integrated circuit comprising:

a plurality of modules having their operations controlled by respective chip select signals, wherein

~~said~~ each ~~module~~ of said modules has a plurality of memory cells; ~~and~~

~~said~~ each ~~module~~ of said modules has a control circuit controlling an operation of reading or writing data from or into said memory cell, respectively,

said plurality of modules receive a common address signal sent through a common internal address bus, ~~where~~

said plurality of modules have a different number of word lines ~~different in number~~ from each other such that one of said plurality of modules has a finite maximum number of word lines, and

said control circuit included in ~~a module~~ one of said modules that does not have ~~a~~ the maximum number of word lines among said plurality of modules controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of said chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values.

4. (Previously Presented) The semiconductor integrated circuit according to claim 3, wherein

said prescribed bits are used in specifying a word line of a module having a maximum number of word lines and are not used in specifying a word line of said module that does not have a maximum number of word lines.

5. (Canceled)

6. (Original) The semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a redundancy circuit in a column.

7. (Currently Amended) The semiconductor integrated circuit according to claim 6, wherein said error register outputs held error data when an address signal indicates a prescribed value,

said semiconductor integrated circuit further ~~comprising~~ comprises a repair code generation circuit receiving said error data for generating a repair code for repairing a defective memory cell array using said redundancy circuit.

8. (Original) The semiconductor integrated circuit according to claim 7 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register; and

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector.

9. (Original) The semiconductor integrated circuit according to claim 6 comprising:

a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element;

a register holding a repair code;

a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register;

a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector; and

a processor controlling an execution of a two-step test, wherein

said processor controls writing of test data into a memory cell and reading of test data from a memory cell without causing said repair control circuit to perform repair in a first step of the test,

generates a repair code corresponding to error data stored in said error register in said first step of the test for storage into said register, and

controls writing of test data into a memory cell and reading of test data from a memory cell while allowing said selector to output the repair code from said register to cause said repair control circuit to perform the repair.